[0078] A p-base layer **5***s* is formed around the trench contact **17***s*. Near the bottom of the trench contact **17***s*, a p^+-contact layer **7***s* is formed so as to protrude downward from the p-base layer **5***s*. That is, the lower surface of the p^+-contact layer **7***s* is located lower than the lower surface of the p-base layer **5***s*. As viewed from above, the p-base layer **5***s* and the p^+-contact layer **7***s* are shaped like a frame along the trench contact **17***s*.

[0079] On the other hand, the lower surface of the outer peripheral portion of the field plate electrode **13** is shaped like a staircase, with its lower surface ascending toward the outer periphery. Also directly below the field plate electrode **13**, n-pillar layers **3** and p-pillar layers **4** are formed, constituting a superjunction structure.

[0080] In this embodiment, a frame-shaped p-base layer **5***s* is formed in the device termination section. The p-base layer **5***s* does not have a MOS gate structure, but includes a wide contact along with the p^+-contact layer **7***s* for discharging holes generated in the termination section. Along the frame-shaped p-base layer **5***s*, a frame-shaped trench **16***s* is formed concentrically with the p-base layer **5***s*, and a trench contact **17***s* is buried in the trench **16***s*. Thus holes can be efficiently discharged from the device termination section to enhance the breakdown voltage of the termination section.

[0081] The trench **16***s* in the termination section has a wider width than the trench **16** in the cell section. For process-related reasons, the trench deepens as its width increases. Hence the p^+-contact layer **7***s* is located slightly deeper than the p^+-contact layer **7** in the cell section. Thus holes in the termination section are discharged more easily, and higher withstand capability can be achieved.

[0082] If the p^+-contact layer **7***s* is formed at a deeper position, the drift layer for holding the breakdown voltage is thinned accordingly. Hence the breakdown voltage may decrease contrarily. Thus it is preferable that the impurity concentration in the n-pillar layer **3** and the p-pillar layer **4** formed in the termination section be lower than in the pillar layers of the cell section having the MOS gate structure.

[0083] Furthermore, in this embodiment, the p-base layer **5***s* is curved at the corners of the device. This can prevent electric field concentration at the edge of the p-base layer **5***s*. Moreover, the p^+-contact layer **7** is curved concentrically with the p-base layer **5**. Hence holes can be discharged equally rapidly at any portion of the corner.

[0084] Furthermore, in this embodiment, the lower surface of the outer peripheral portion of the field plate electrode **13** is shaped like a staircase. This can prevent electric field concentration at a particular corner of the field plate electrode **13**. Thus the breakdown voltage can be further enhanced. The configuration, operation, and effect in this embodiment other than the foregoing are the same as those in the first embodiment described above.

[0085] Next, a first variation of the sixth embodiment is described.

[0086] FIG. **14** is a cross-sectional view schematically illustrating a power MOSFET according to this variation.

[0087] As shown in FIG. **14**, in this variation, the p^+-contact layers **7** and **7***s* are formed to entirely cover the side face of the trench contacts **17** and **17***s*, respectively. Thus, by forming the p^+-contact layer **7***s* also on the sidewall of the trench **16***s* in the termination section, holes flowing in the surface of the semiconductor layer in the termination section can be rapidly discharged, and higher withstand capability can be achieved. The configuration, operation, and effect in this variation other than the foregoing are the same as those in the sixth embodiment described above.

[0088] Next, a second variation of the sixth embodiment is described.

[0089] FIG. **15** is a cross-sectional view schematically illustrating a power MOSFET according to this variation.

[0090] As shown in FIG. **15**, in this variation, a plurality of trenches **16***s* are formed concentrically in the termination section. The width of each trench **16***s* is equal to the width of the trench **16** in the cell section. Hence the depth of the trench **16***s* can be equalized to the depth of the trench **16**. Thus, in this variation, a plurality of trench contacts **17***s* are formed concentrically in the termination section, and the width and depth of each trench contact **17***s* are equal to the width and depth of the trench contact **17** in the cell section.

[0091] According to this variation, the thickness of the drift layer in the termination section can be equalized to that in the cell section. Thus the decrease of breakdown voltage in the termination section can be prevented more definitely. The configuration, operation, and effect in this variation other than the foregoing are the same as those in the sixth embodiment described above.

[0092] In the sixth embodiment and its first and second variation, the field plate electrode **13** is illustratively connected to the source electrode **10**. However, the invention is not limited thereto, but the field plate electrode may be connected to the gate electrode. Furthermore, the termination structure based on the RESURF structure or the guard ring structure is also practicable. Moreover, the sixth embodiment and its first and second variation illustrate a configuration where the superjunction structure is formed also outside the p-base layer **5***s* in the termination section. However, the superjunction structure may be omitted in this portion.

[0093] The invention has been described with reference to the first to sixth embodiment and their variations. However, the invention is not limited to these embodiments and the like. For example, in the description of the above embodiments, it is assumed that the first conductivity type and the second conductivity type are n-type and p-type, respectively. However, it is also practicable that the first conductivity type and the second conductivity type are p-type and n-type, respectively. Furthermore, the planar pattern of the MOS gate section and the superjunction structure is not limited to the striped configuration, but may be formed in a lattice or staggered configuration, for example.

[0094] Furthermore, the p-pillar layer **4** may be in contact with the n^+-drain layer **2**. Also in this case, the same effect as in the above embodiments is achieved. It is likewise practicable that a layer having a lower impurity concentration than the n-pillar layer **3** is inserted between the superjunction structure and the n^+-drain layer **2**.

[0095] Moreover, the above embodiments and variations can be practiced in combination. For example, in the sixth embodiment and its first and second variation (see FIGS. **12** to **14**), the cell section illustratively has the same configuration as the first embodiment (see FIG. **1**) or its second variation (see FIG. **3**). However, the invention is not limited thereto, but the sixth embodiment and its first and second variation can be practiced in combination with any other embodiment or variation.

[0096] In the description of the above embodiments and variations, silicon (Si) is used as the semiconductor in the MOSFETs. However, compound semiconductors such as